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18ES51

Fifth Semester B.E. Degree Examination, July/August 2021
Technological Innovation Management and Entrepreneurship

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

1 a. Define Management. List and explain the essential management functions. **(08 Marks)**
b. Explain the various roles of a Manager. **(07 Marks)**
c. Compare 'management' with administration. **(05 Marks)**

2 a. With a neat diagram, explain the hierarchy of organizational plans. **(08 Marks)**
b. Explain the various steps involved in rational decision making with a neat diagram. **(08 Marks)**
c. Explain any five limitations of planning. **(04 Marks)**

3 a. Explain about the purpose of organization and the process of organizing. **(10 Marks)**
b. What is recruitment? Explain the steps in the selection process. **(10 Marks)**

4 a. Explain Maslow's need hierarchy theory with a neat diagram. **(10 Marks)**
b. Define leadership. Explain briefly about any two leadership styles. **(10 Marks)**

5 a. Describe the social responsibilities of business towards different groups in a society. **(10 Marks)**
b. What is Social Audit? List its benefit and limitations. **(10 Marks)**

6 a. Define Entrepreneurship. Explain the characteristics of an Entrepreneur. **(10 Marks)**
b. Briefly explain the various classifications of Entrepreneurs. **(10 Marks)**

7 a. Briefly explain the importance of the family business and the different stages of development of a family business. **(10 Marks)**
b. Discuss the contribution made by Indian family business with examples. **(10 Marks)**

8 a. Explain the various ways to generate business ideas, and briefly describe how to identify a Business opportunity. **(10 Marks)**
b. Briefly explain about Marketing and financial feasibility analysis. **(10 Marks)**

9 a. List and explain the contents of a Business plans. **(08 Marks)**
b. Why do some Business plans fails? Explain. **(04 Marks)**
c. Define Venture Capital. List out the stages of venture capital financing. **(08 Marks)**

10 a. Explain the importance of Network analysis during project execution. **(08 Marks)**
b. Discuss the steps in CPM network analysis techniques, with its advantages and limitations. **(08 Marks)**
c. Compare PERT with CPM. **(04 Marks)**

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18EC52

Fifth Semester B.E. Degree Examination, July/August 2021
Digital Signal Processing

Time: 3 hrs. Max. Marks: 100

Note: *Answer any FIVE full questions.*

1 a. Describe the process of frequency domain sampling and reconstruction of discrete time signal. **(08 Marks)**

b. Find the 4-point DFT of the sequence $x(n) = \{1, 2, 0, 1\}$ using matrix method. **(04 Marks)**

c. Using graphical method (concentric method) obtain 5 point circular convolution of two DFT signal defined as,

$x(n) = (1.5)^n ; \ 0 \le n \le 2$

$y(n) = (2n-3) ; \ 0 \le n \le 3$ **(08 Marks)**

2 a. Compute the 4-point DFT of the given sequence $x(n) = \{0, 1, 2, 3\}$ and verify the result with IDFT method using formula method. **(08 Marks)**

b. Compute the N-point DF of the sequence $x(n) = a^n ; \ 0 \le n \le N-1$. **(04 Marks)**

c. State and prove the following properties :

(i) Circular time shift of a sequence.

(ii) Parseval's theorem. **(08 Marks)**

3 a. Consider a FIR filter with impulse response $h(n) = \{3, 2, 1, 1\}$, if the I/P $x(n) = \{1, 2, 3, 3, 2, 1, -1, -2, -3, 5, 6, -1, 2, 0, 2, 1\}$ find the output. Use overlap save method assuming the length of the block is 9. **(10 Marks)**

b. Find the 8 point DFT of the sequence $x(n) = \{1, 1, 1, 1, 0, 0, 0, 0\}$ using DIT – FFT radix – 2 algorithm and draw the signal flow graph. **(10 Marks)**

4 a. Consider a FIR filter with impulse response $h(n) = \{1, 2\}$ and input sequence $x(n) = \{1, 4, 3, 0, 7, 4, -7, -7, -1, 3, 4, 3\}$. Compute y(n) using overlap add technique assuming the length of the block is 5. **(10 Marks)**

b. Derive the computational arrangement of 8-point DFT using Radix-2 DIF-FFT algorithm and draw the signal flow diagram. **(10 Marks)**

5 a. Design a symmetric FIR low pass filter whose designed frequency is given by,

$$H_d(\omega) = \begin{cases} e^{-j\omega\tau} & ; |\omega| \le \omega_C \\ 0 & ; \text{otherwise} \end{cases}.$$

The length of the filter should be 7 and cut off frequency is 1 rad/sec use rectangular window. **(08 Marks)**

b. Determine the direct form realization of the following system function:

$H(z) = 1 + 2z^{-1} - 3z^{-2} + 5z^{-4} - 4z^{-3}$. **(06 Marks)**

c. List the advantages and disadvantages of FIR filters. **(06 Marks)**

6 a. Draw the magnitude response and show the biggest side lobe values for the following windows:
(i) Rectangular window. (ii) Hanning window.
(iii) Hamming window. (iv) Bartlett window **(04 Marks)**

b. The desired frequency response of a low pass filter is given by,

$$H_d(e^{j\omega}) = H_d(\omega) = \begin{cases} e^{-j3\omega}; & |\omega| < \frac{3\pi}{4} \\ 0 & ; \frac{3\pi}{4} < |\omega| < \pi \end{cases}$$

. Determine the frequency response of the FIR filter if Hamming window is used with N = 7. **(08 Marks)**

c. Consider an FIR lattice filter with coefficients $K_1 = 0.65$, $K_2 = -0.34$, $K_3 = 0.8$, find its impulse response. Draw the equivalent direct form structure. **(08 Marks)**

7 a. Draw the frequency response curve and write the transformation to convert the analog lowpass prototype into practical analog low pass, high pass, band pass and band stop filters with specified frequency. **(08 Marks)**

b. Realize the following digital filter using a direct form II structure

$$H(z) = \frac{1 + 0.4z^{-1}}{1 - 0.5z^{-1} + 0.06z^{-2}}.$$ **(04 Marks)**

c. Assuming that T = 2 sec in BLT and given the following points:
(i) $S = -1 + j$, on the left half of the S-plane.
(ii) $S = 1 - j$, on the right half of the S-plane.
(iii) $S = j$, on the positive jw on the S-plane.
(iv) $S = -j$ on the negative jw on the S-plane.
Convert each of these points in the S-plane to the Z-plane and verify the mapping properties. **(08 Marks)**

8 a. Draw and discuss flow chart for IIR filter design using Bilinear transformation. **(04 Marks)**

b. An analog filter is given by,

$$H_a(s) = \frac{3}{(s+3)(s+1)},$$

with T = 1 sec. Obtain H(z) using Bilinear transformation. **(08 Marks)**

c. Draw the Direct form – I and Direct form – II structure for the system given by,

$$H(z) = \frac{z^{-1} - 3z^{-2}}{(10 - z^{-1})(1 + 0.5z^{-1} + 0.5z^{-2})}$$ **(08 Marks)**

9 a. Explain Digital Signal processors using Harvard architecture. **(08 Marks)**

b. Convert the following number in the IEE single precision format to the decimal format:
(i) 110000000.010.....0000
(ii) 010000000000.....0000 **(04 Marks)**

c. Explain Fixed-point digital signal processes using basic architecture of TMS320C54X family. **(08 Marks)**

10 a. Explain the following Digital Signal processor hardware units:
(i) Multiplier and Accumulator
(ii) Shifters
(iii) Address Generators. **(09 Marks)**

b. Discuss IEEE Double Precision format. **(07 Marks)**

c. Convert the following Q-15 signed numbers into the Decimal number :
(i) 1110101110000010
(ii) 0100011110110010 **(04 Marks)**

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18EC53

Fifth Semester B.E. Degree Examination, July/August 2021
Principles of Communication Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain in detail, the working of switching modulator with suitable block diagram and necessary derivations. **(08 Marks)**

b. Using the message signal $M(t) = \frac{1}{(1+t^2)}$. Determine and sketch the modulated wave for amplitude modulation with the following values : i) $\mu = 50\%$ ii) $\mu = 100\%$. **(06 Marks)**

c. Explain the concept of VSB transmission for analog and digital transmission. **(06 Marks)**

2 a. Derive an equation for SSB modulated wave for which upper sideband is retained. **(07 Marks)**

b. Explain how Costas receiver is used for demodulating DSB – SL signal. **(07 Marks)**

c. With relevant block diagram, explain the working of FDM transmitter and receiver. **(06 Marks)**

3 a. Derive the equation of frequency modulated wave. Define :
i) Modulation index
ii) Maximum deviation of frequency modulated single. **(06 Marks)**

b. With neat circuit diagram, explain FM demodulation using balanced slope detector. **(07 Marks)**

c. With a neat block diagram, explain the concept of super hetero dyne receiver. **(07 Marks)**

4 a. With relevant diagram, explain direct method generation of FM using Hartley oscillator and how frequency stability is achieved. **(08 Marks)**

b. When a 50.4MHz carrier is frequency modulated by a sinusoidal AF modulating signal. The highest frequency reached is 50.405MHz. Calculate :
i) Frequency deviation produced
ii) Carrier swing of the wave
iii) Lowest frequency reached. **(06 Marks)**

c. Explain the linear model of PLL using relevant diagram and suitable expressions. **(06 Marks)**

5 a. Explain shot noise and thermal noise with relevant diagrams and expressions. **(06 Marks)**

b. Show that the figure of merit for DSBSC system is unity using suitable expressions. **(08 Marks)**

c. Why Preemphasis and Deemphasis are required. Explain how they are implemented. **(06 Marks)**

6 a. What is White Noise? Explain the power spectral density and auto correlation function. **(07 Marks)**

b. The average noise per unit BW measured at the front end of the AM receiver is 10^{-3}W/Hz. The modulated wave is sinusoidal with a carrier power of 80KW and side band power of 10KW per side band. The message band width is 4KHz. Determine the SNR_0 of the system and FOM(Figure of Merit). **(06 Marks)**

c. Explain about FM threshold effect and its reduction method. **(07 Marks)**

7 a. What are the advantages of digital signal over analog signal? **(04 Marks)**
b. State and prove sampling theorem for band limited signals. **(08 Marks)**
c. With neat block diagram, explain the generation of PPM waves. **(08 Marks)**

8 a. With neat block diagram, explain the generation PAM waves. **(08 Marks)**
b. Describe the effect of noise in pulse position modulation. **(06 Marks)**
c. Explain the working of TDM system with necessary block diagram. **(06 Marks)**

9 a. Explain the construction and regeneration of PCM signal. **(10 Marks)**
b. Explain the construction of Delta modulation signal. **(06 Marks)**
c. Write short notes on vocoder. **(04 Marks)**

10 a. What is quantization noise? Derive the output signal to noise ratio of the uniform quantizer. **(07 Marks)**
b. To transmit a bit sequence 10011011. Draw the resulting waveform using :
i) Unipolar NRZ ii) Polar NRZ iii) Unipolar RZ
iv) Bipolar RZ v) Manchestor (split phase). **(06 Marks)**
c. Explain how digitization of video and MPEG is achieved with relevant diagram. **(07 Marks)**

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18EC54

Fifth Semester B.E. Degree Examination, July/August 2021
Information Theory and Coding

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions.

1 a. Define the following with respect to information theory:
(i) Self information (ii) Entropy
(iii) Rate of information (iv) Source efficiency **(04 Marks)**

b. Find the relationship between Hartley's nats and bits. **(06 Marks)**

c. Consider the Markov source shown in Fig.Q1(c). Find:
(i) State probabilities (ii) State entropies (iii) Source entropy

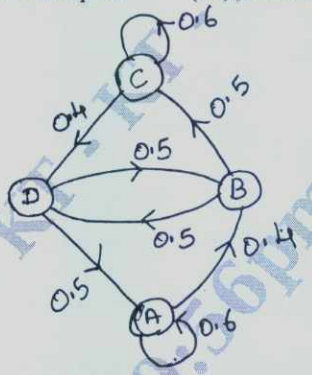

Fig.Q1(c) **(10 Marks)**

2 a. A source emits one of the four probable messages m_1, m_2, m_3, m_4 with probabilities of 7/16, 5/16, 1/8 and 1/8 respectively. Find the entropy of the source. List all the elements for the second extension of this source. Hence show $H(s^2) = 2H(s)$. **(08 Marks)**

b. Prove extremal property of entropy. **(06 Marks)**

c. In a facsimile transmission of picture, there are about 2.25×10^6 pixel frame. For a good reproduction 12 brightness levels are necessary. Assume all these levels are equally likely to occur. Find the rate of information if one picture is to be transmitted every 3 minitus. What is the source efficiency of this facsimile transmitter? **(06 Marks)**

3 a. Define non-singular and uniquely decidable codes with an example. **(04 Marks)**

b. A source emits an independent sequence of symbols from an alphabet consisting of five symbols A, B, C, D and E with probabilities of ¼, 1/8, 1/8, 3/16 and 5/16 respectively. Find the Shannon code for each symbol and efficiency of the coding scheme. **(10 Marks)**

c. State and prove Shannon's first theorem. **(06 Marks)**

4 a. State Prefix and Kraft McMillan inequality property. **(04 Marks)**

b. A source produces nine symbols x_1, x_2.....x_9 with respective probabilities of 0.24, 0.23, 0.19, 0.13, 0.08, 0.06, 0.04, 0.02 and 0.01.
(i) Construct a Shannon-Fano ternary code.
(ii) Determine the code-efficiency and redundancy.
(iii) Draw code-tree.
(iv) Determine the probabilities of 0, 1 and 2 when the encoding alphabet is {0, 1, 2}. **(10 Marks)**

c. Find the minimum number of symbols 'r' in the coding alphabet for devising an instantaneous code such that w = {0, 5, 0, 5, 5}. Device such a code.
(Note: w represents the set of code words of length 1, 2, 3....) **(06 Marks)**

5 a. Show that $H(X,Y) = H\left(\frac{X}{Y}\right) + H(Y)$. **(04 Marks)**

b. A non-symmetric binary channel is given in Fig.Q5(b).

(i) Find H(X), H(Y), $H\left(\frac{X}{Y}\right)$ and $H\left(\frac{Y}{X}\right)$ given $P(X = 0) = \frac{1}{4}$, $P(X = 1) = \frac{3}{4}$, $\alpha = 0.75$, $\beta = 0.9$.

(ii) Find the capacity of the binary symmetric channel if $\alpha = \beta = 0.75$.

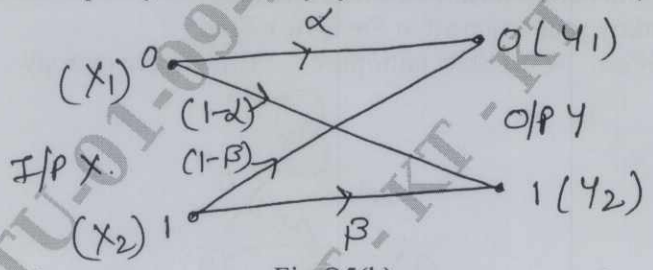

Fig.Q5(b) **(10 Marks)**

c. Show that the mutual information of a discrete channel is symmetric. **(06 Marks)**

6 a. Derive an expression for channel capacity of binary Erasure channel. **(08 Marks)**

b. For the JPM given below, compute individually H(X), H(Y), H(X, Y), $H\left(\frac{X}{Y}\right)$, $H\left(\frac{Y}{X}\right)$ and I(X, Y).

$$P(X,Y) = \begin{bmatrix} 0.05 & 0 & 0.20 & 0.05 \\ 0 & 0.10 & 0.10 & 0 \\ 0 & 0 & 0.20 & 0.10 \\ 0.05 & 0.05 & 0 & 0.10 \end{bmatrix}$$ **(08 Marks)**

c. What is joint probability matrix? State its properties. **(04 Marks)**

7 a. Define Hamming weight, Hamming distance and minimum distance of linear block codes (with example). **(06 Marks)**

b. For a systematic (7, 4) linear block code, the parity matrix P is given by

$$[P] = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}$$

(i) Find G and H.
(ii) Draw the encoding circuit.
(iii) Find all possible valid code vectors.
(iv) A single error has occurred each of these received vectors. Detect and correct those errors. (1) RA = [0111110] (2) RB = [1011100]
(v) Draw the syndrome calculation circuit. **(14 Marks)**

8 a. The generator polynomial of a (15, 7) cyclic code is given by $g(x) = 1 + x^4 + x^6 + x^7 + x^8$.
(i) Draw the syndrome calculation circuit.
(ii) Find the syndrome of the received polynomial $z(x) = 1 + x + x^3 + x^6 + x^8 + x^9 + x^{11} + x^{14}$ by listing the states of the register used in syndrome calculation circuit.
(iii) Verify the syndrome obtained in (ii) by using direct hand calculation. **(10 Marks)**

b. Consider the (15, 11) cyclic code generated by $g(x) = 1 + x + x^4$.
(i) Draw the feedback register encoding circuit for this cyclic code.
(ii) Illustrate the encoding procedure with the message vector 01101001011 by listing the state of the register with each input.
(iii) Verify the code polynomial by using the division method. **(10 Marks)**

9 a. What are convolutional codes? How it is different from block codes. **(05 Marks)**

b. Consider the convolutional encodes shown in Fig.Q9(b).
(i) Find the O/P for the message 10011 using time domain approach.
(ii) Find the O/P for the message 10011 using transform domain approach.

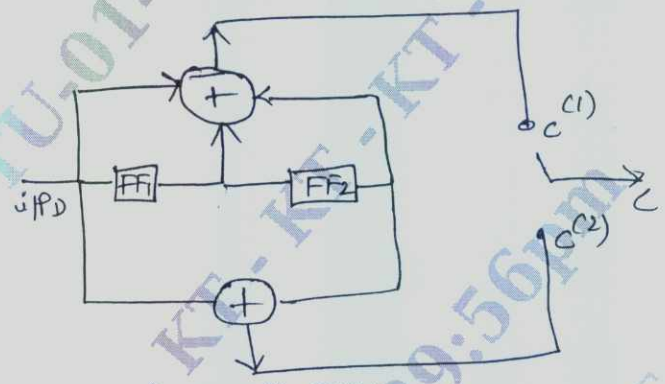

Fig.Q9(b) **(10 Marks)**

c. What do you understand by trellis diagram of a convolutional encodes? Explain clearly. **(05 Marks)**

10 a. For (2, 1, 3) convolution encodes with g(1) = 1011, g(2) = 1101.
(i) Write translation table.
(ii) State diagram.
(iii) Draw the code tree.
(iv) Draw the trellis diagram.
(v) Find the encoded O/P for the message 11101 by traversing the code tree. **(15 Marks)**

b. Explain Viterbi encoding. **(05 Marks)**

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18EC56

Fifth Semester B.E. Degree Examination, July/August 2021
Verilog HDL

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Explain the various stages used in VLSI design with a neat flow diagram. **(08 Marks)**

b. Design a 4-bit ripple carry counter using a top-down design methodology. **(08 Marks)**

c. Compare the HDL programming to traditional software programming. **(04 Marks)**

2 a. Give the importance of stimulus block. Explain the different styles of stimulus block used for testing the design. **(08 Marks)**

b. Explain the different levels of abstraction. **(06 Marks)**

c. Write a pseudo verilog code for 4-bit ripple carry adder with following description.

i) Define a module FA with input A, B C in, sum and carry with no internals.

ii) Instantiate 4 full adders of the type FA in the module Ripple-Add and name them as FA0, FA1, FA2 and FA3. **(06 Marks)**

3 a. Illustrate with examples the data types used to define nets, registers, vectors and arrays. **(08 Marks)**

b. Differentiate i) $display and$ monitor ii) $stop and $finish with examples. **(06 Marks)**

c. Declare a top-level module as TOP for stimulus. Define a constant N of size 8, IN_REG (8 bit) LOAD_EN(1-bit), LOAD_VAL (8-bit) and CLK(1bit) as register variables, and OUI_ REG (8-bit) as wire. Instantiate the module shift_reg and call it as SRl. Connect the port by named list. **(06 Marks)**

4 a. Illustrate with example the post connection rule of verilog HDL programming. **(08 Marks)**

b. Draw the logic diagram of SR latch. Develop the verilog code for SR latch. Identify the components and hence write the test bench to verify the functionality. **(08 Marks)**

c. Declare the following variables in verilog.

i) Net 'A is fixed to logic value '0' at declaration

ii) Vector register, Address_bus of 41 bit wide

iii) A memory MEM containing 256 words of 64 bit each

iv) An integer called count. **(04 Marks)**

5 a. Design a 4-bit ripple carry full adder using 1-bit full adder. Develop the verilog code for a 4-bit ripple carry full adder using gate level modeling. Verify the functionality with appropriate test bench. **(08 Marks)**

b. Given A = 5'b10101 ; B = 5'b11101 ; C = 5'b11001 ; D = 5'b10011. Evaluate.

i) Y = A & B ii) Y = ~ (& C) iii) Y = C ^ D

iv) Y = C% A v) Y = A + (D>>>1) vi) Y = {B[3], C[2], A} **(06 Marks)**

c. Discuss the gate delays along with its types of delay specification. **(06 Marks)**

6 a. Design a 4-bit ripple carry counter using TFF. Write the verilog code using data flow modeling. Verify the code with appropriate test bench. **(08 Marks)**

b. Design a 2×1 MUX using bufif0 and bufif1 gates. Write the verilog code using gate level modeling for the given delay specification.

	Min	Max	Typ
Rise	1	3	2
Fall	3	5	4
Turnoff	5	7	6

(06 Marks)

c. Discuss the types of delays used in the continuous assignment statement. **(06 Marks)**

7 a. i) Differentiate blocking and non-blocking statement with appropriate examples.
ii) Design a clock with period 40 and a duty cycle of 25% by using the always and initial statement. The value of clock at time = 0 is initialized to 0. Display the value. **(08 Marks)**

b. Design a 4×1 MUX and develop a verilog code using case statement. **(06 Marks)**

c. Bring out the differences and similarities between task and function. **(06 Marks)**

8 a. Compare sequential and parallel block with appropriate example. **(06 Marks)**

b. Define a task to compute the parity of a 16-bit data. Write a verilog code to call task calc-parity to compute the parity. Display the message as even or odd parity. **(08 Marks)**

c. Discuss the for loop and forever statement with example. **(06 Marks)**

9 a. Illustrate with examples the system tasks related to files. **(06 Marks)**

b. Write a verilog program for a positive edge triggered DFF with asynchronous clear (q = 0) and preset (q = 1) using assign and deassign statements. **(06 Marks)**

c. Give the importance of parameter overriding. Explain the two techniques of parameter overriding with examples. **(08 Marks)**

10 a. List the limitation of manually obtained gate level synthesis of design. How these are analyzed and addressed using automated logic synthesis tools. **(08 Marks)**

b. Discuss in detail the steps involved in the logic synthesis flow from RTL to gates with a neat flow diagram. **(08 Marks)**

c. Interpret the gatelevel netlist diagram for the following when run on a synthesis tool.
i) assign out = (Sel)? I1 : I0 ;
ii) always @ (posedge clk)
q⇐d ;
(04 Marks)

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